Amendments to the Claims

The following listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

Claims 1-32 (Canceled)

33. (New) A network of computing devices comprising:

a. a digital computer which is:

i. capable of operating as an initiator digital computing device for a Small Computer System Interface ("SCSI") bus; and

ii. connected in parallel to a first SCSI bus;

b. a SCSI bus repeater which includes:

i. a first interface that is connected to the first SCSI bus for receiving signals therefrom and supplying signals thereto;

ii. a second interface that is connected to a second SCSI bus for receiving signals therefrom and supplying signals thereto; and

iii. a control circuit for controlling operation of the first and second SCSI bus interfaces that:

A) permits a succession of SCSI bus phases initiated by an initiator digital computing device that is connected to either of the SCSI buses to be concluded by a target digital computing device

connected to the other SCSI bus, the succession of SCSI bus phases ending upon occurrence of a bus free phase of the SCSI buses; and

B) during the succession of SCSI bus phases, the control circuit, responsive to at least a first signal present at least one of the first and second interfaces, controlling at least a second signal coupled from at least one of the interfaces to the SCSI bus to which the interface connects; and

c. a target digital computing device connected in parallel to the second SCSI bus.

34. (New) The network of computing devices of claim 33 wherein the control circuit of the SCSI bus repeater:

during the succession of SCSI bus phases stores information which identifies the SCSI bus to which the digital computing device which initiated the succession of SCSI bus phases connects; and

uses the information so stored in controlling a signal supplied from at least one of the interfaces to one of the signal lines of the SCSI bus connected to the interface other than the BSY signal line of that SCSI bus.

35. (New) The network of computing devices of claim 33 wherein the control circuit of the SCSI bus repeater stores

information which identifies individual phases in the succession of SCSI bus phases.

36. (New) A network of computing devices comprising:

a. a digital computer which is connected in parallel to a sharing distributed arbitration digital data bus;

b. a repeater for exchanging information between digital computing devices respectively connected in parallel to the sharing distributed arbitration digital data bus or to a shared distributed arbitration digital data bus, said repeater interconnecting the shared and the sharing distributed arbitration digital data buses into a single, composite distributed arbitration digital data bus, said repeater including:

i. a shared bus interface circuit, connected to the shared distributed arbitration digital data bus, for receiving signals from and transmitting signals to a device connected to the shared distributed arbitration digital data bus;

ii. a sharing bus interface circuit, connected to the sharing distributed arbitration digital data bus, for receiving signals from and transmitting signals to a device connected to the sharing distributed arbitration digital data bus; and

iii. control circuit, simultaneously connected both to said shared bus interface circuit and to said sharing bus

interface circuit, said control circuit responding to a plurality of signals on the shared and sharing distributed arbitration digital data buses for controlling both of said bus interface circuits during an exchange of information between devices connected to the composite distributed arbitration digital data bus; and

c. a digital computing device connected in parallel to the sharing distributed arbitration digital data bus.

37. (New) The network of computing devices of claim 36 wherein information is exchanged between devices connected to the composite distributed arbitration digital data bus in accordance with a bus protocol having a plurality of phases, said control circuit of said repeater also responding to an occurrence of a sequence of phases of the bus protocol.

38. (New) The network of computing devices of claim 37 wherein the shared distributed arbitration digital data bus employs a first signaling convention for communicating signals thereon and the sharing distributed arbitration digital data bus employs a second signaling convention for communicating signals thereon, the first and second signaling conventions by which signals are communicated respectively on the shared and sharing distributed arbitration digital data buses being incompatible with each other.

39. (New) The network of computing devices of claim 37 wherein said shared bus interface circuit of said repeater exchanges signals with a device in accordance with a first signaling convention, said shared bus interface circuit of said repeater indicating if a device employing a different signaling convention, incompatible with the first signaling convention of said shared bus interface circuit of said repeater, is connected to the shared distributed arbitration digital data bus.

40. (New) The network of computing devices of claim 37 wherein said sharing bus interface circuit of said repeater exchanges signals with a device in accordance with a first signaling convention, said sharing bus interface circuit of said repeater indicating if a device employing a different signaling convention, incompatible with the first signaling convention of said sharing bus interface circuit, is connected to the sharing distributed arbitration digital data bus.

41. (New) A network of computing devices comprising:

a. a digital computer which is:

i. capable of operating as an initiator digital computing device for a SCSI bus; and

ii. connected in parallel to a first SCSI bus;

b. a repeater for exchanging information between an initiator digital computing device that connects in parallel to the first SCSI bus and a target digital computing device that

connects in parallel to a second SCSI bus, each SCSI bus respectively including signal lines via which the initiator and target digital computing device exchange signals, said repeater interconnecting the first and the second SCSI buses into a single, composite SCSI bus, said repeater including:

i. first SCSI bus interface circuit, connected to the first SCSI bus, for receiving signals from and transmitting signals to the initiator digital computing device;

ii. second SCSI bus interface circuit, connected to the second SCSI bus, for receiving signals from and transmitting signals to a target digital computing device; and

iii. control circuit, simultaneously coupled both to said first SCSI bus interface circuit and to said second SCSI bus interface circuit, for controlling said first and second SCSI bus interface circuits during a sequence of SCSI bus phases that commences when an initiator digital computing device, during a BUS FREE phase of the SCSI bus protocol, initiates an ARBITRATION phase of the SCSI protocol; during the sequence of SCSI bus phases commenced by the initiator digital computing device the control circuit controlling the signal present on at least one signal line of either the first or second SCSI buses responsive to a signal present on a different signal line of either the first or second SCSI buses; and the sequence of SCSI bus phases ending whenever a BUS FREE phase of the SCSI bus protocol occurs; and

c. a target digital computing device connected in parallel to the second SCSI bus.

42. (New) The network of computing devices of claim 41 wherein the control circuit of the repeater stores information that identifies the SCSI bus to which the initiator device connects, the control circuit responsive to the stored information controlling the signal present on at least one signal line of either the first or second SCSI buses other than a Select ("SEL") signal line thereof.

43. (New) The network of computing devices of claim 41 wherein the control circuit of the repeater during one phase in the sequence of SCSI bus phases stores information for use during a subsequent phase in the sequence of SCSI bus phases.